IS 7412 (1974): Life testing of semiconductor devices [LITD 5: Semiconductor and Other Electronic Components and Devices]

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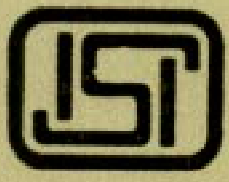
IS : 7412 - 1974
(Reaffirmed 2006)

Indian Standard
LIFE TESTING OF SEMICONDUCTOR DEVICES

UDC 621·382·2/·3 : 620·169·1



INDIAN STANDARDS INSTITUTION
MANAK BHAVAN, 9 BAHADUR SHAH ZAFAR MARG
NEW DELHI 110001

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Indian Standard
LIFE TESTING OF SEMICONDUCTOR DEVICES

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Indian Standard
LIFE TESTING OF SEMICONDUCTOR DEVICES

0. FOREWORD

0.1 This Indian Standard was adopted by the Indian Standards Institution on 12 August 1974, after the draft finalized by the Semiconductor Devices and Integrated Circuits Sectional Committee had been approved by the Electrotechnical Division Council.

0.2 This standard deals with the life test procedure for semiconductor devices applicable for approval purposes (type-approval and acceptance sampling) as well as for reliability evaluation. It also includes recommended electrical conditions and circuit details for different device categories for facilitating easy comparison of data for approval and reliability purposes presented by different manufacturers.

0.2.1 Test procedures for environmental conditions (climatic and mechanical durability) are covered in IS : 6553-1971*.

0.3 Type approval procedure and sampling scheme for acceptance purposes are also described in Appendices A and B respectively for ease of reference and for application of the life test covered in this standard.

0.4 This standard is largely based on IEC Doc : 47 (C.O) 437 'Essential ratings and characteristics — electrical tests for acceptance and reliability' issued by the International Electrotechnical Commission.

0.5 This standard is one of a series of Indian Standards on semiconductor devices and integrated circuits. A list of standards so far prepared in this series is given on page 16.

0.6 For the purpose of deciding whether a particular requirement of this standard is complied with, the final value, observed or calculated, expressing the result of a test, shall be rounded off in accordance with IS : 2-1960†. The number of significant places retained in the rounded off value should be the same as that of the specified value in this standard.

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*Environmental requirements for semiconductor devices and integrated circuits.

†Rules for rounding off numerical values (*revised*).

1. SCOPE

1.1 This standard deals with life test procedure for semiconductor devices applicable for the following purposes:

a) Type approval or type testing,
b) Acceptance testing, and
c) Reliability evaluation.

2. TERMINOLOGY

2.1 For the purpose of this standard, the terms and definitions specified in IS : 2500 (Part I)-1963* and IS : 2612-1965† shall apply.

3. CONDITIONS FOR TESTING

3.1 Standard Atmospheric Conditions

3.1.1 All measurements of the characteristics shall be carried out under the following conditions:

Temperature	25 ± 3°C
Relative humidity	45 to 75 percent
Air pressure	860 to 1 060 mbar

3.1.2 Reference measurements shall be carried out under the following conditions:

Temperature	25 ± 1°C
Relative humidity	50 ± 2 percent
Air pressure	860 to 1 060 mbar

3.2 Mode of Operation — The device should be operated under steady state (ac or dc as appropriate) conditions. In some cases, intermittent operation or other modes of operations may be necessary for supplementary tests.

3.3 Mounting of the Devices

3.3.1 *Ambient Rated Devices* — Unless otherwise specified, the free lead length between case and electrical contacts or supports should be not less than 5 mm for single-ended or for double-ended devices. Devices with lead length less than 5 mm should be mounted in accordance with the manufacturer's recommendations. The supports shall be at a temperature not lower than the ambient temperature.

*Sampling inspection tables: Part I Inspection by attributes and by count of defects.

†Recommendation for type approval and sampling procedures for electronic components.

3.3.2 *Case Rate Devices* — Provisions shall be made which assure that the specified case temperature is maintained.

3.4 Operating Temperature of the Device (*See* Fig. 1)

3.4.1 The operating temperature at the reference point should preferably be specified at a point between t_{br} and t, t being the temperature at the specified point between t_{br} and t_{Max} corresponding to the 20 percent point.

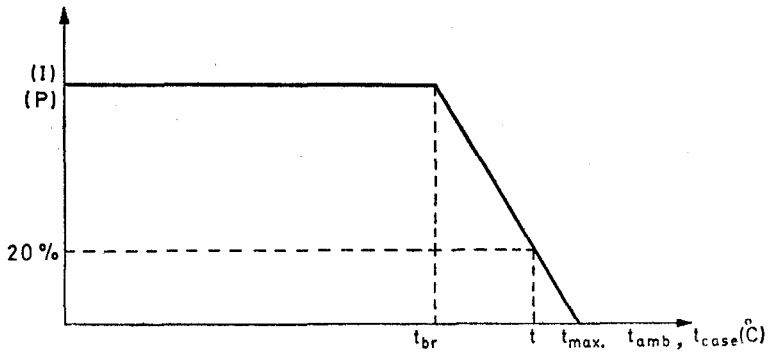


FIG. 1 OPERATING TEMPERATURE

3.4.2 This operating temperature may preferably be reached partly by dissipation (*see* **3.6**) of the device and partly by the ambient temperature.

3.4.3 The operating temperature as specified in relevant individual specification shall be maintained within ± 5°C for ambient rated devices. For the case rated devices, the average of the temperatures of the cases shall be maintained within ± 5°C and any individual case temperature shall be maintained within ± 10°C of the specified operating point.

3.5 Operating Voltages — The operating voltage should be that specified in Table 1 except when otherwise stated in the relevant individual specification. However in no case the absolute maximum rating of the device shall be exceeded. Initial tolerances and any variation during operation shall be within ± 5 percent for dc voltages and ± 10 percent for ac or pulse voltages.

3.5.1 Where there is a requirement for additional tests under conditions different from those specified in Table 1, the combination given in **3.8** should be used.

3.6 Power Dissipation or Current — The devices under test shall be operated within the power dissipation or current according to the derating curve as given in the detailed specification. However in no case the absolute

maximum rating of the device shall be exceeded. Initial tolerance and any variation during operation shall be within ± 5 percent for dc power or current and ± 10 percent for ac or pulse power or current.

3.6.1 Where there is a requirement for additional tests under conditions different from these specified in Table 3, the combinations given in **3.8** should be used.

3.7 Test Circuit and Test Condition — The test circuit and the test condition shall be as specified in Table 1, except when otherwise stated in the relevant individual specification.

3.8 Additional Tests — If an indication of the number of failures or the variation in failure rate with operating conditions is needed, the following combinations of voltage and power dissipation or current are recommended:

Operating Voltage, Percent	*Power Dissipation or Current, Percent*
100	50
	20
50	100
	50
	20
20	100
	50

NOTE 1 — The 100 percent values refer to those specified in Table 1.

NOTE 2 — Some stress combination listed above may not be safely applied to some device classes or types. Any specified test conditions shall be chosen to be within the safe operating area (according to thermal runaway or secondary breakdown or both) for the type of the device under test.

4. DURATION OF LIFE TEST

4.1 Duration of the life test shall be selected from Table 2. If intermediate measurements are made, they shall also be performed at the time intervals given in the table up to 2 000 hours and then after every 2 000 $^{+48}_{-30}$ hours until the required duration has elapsed.

4.1.1 Measurements shall be made as near as possible to this specified time but may be adjusted so that the measurements need not be made during other than normal working days.

4.2 Where the duration of life test is defined by a number of cycles, the sequence 1, 2, 5×10^n, where n is an integer (including zero) shall be used.

5. LIFE TESTING

5.0 The life test shall be conducted on devices which had passed all other relevant tests.

5.1 The selected samples shall be subjected to life tests under conditions specified in **7** for duration selected in accordance with **4**.

NOTE — The failure rate of semiconductor devices is known to decrease with time after a short initial period of high failure rate corresponding to infant mortality period. Advantage of this property is usually taken in reducing the test duration for type approval testing and batch sample testing. For example, unless otherwise specified in the relevant individual specification, a duration of 1 000 hours is usually stipulated for life testing for type approval purposes and a duration of 336 hours for life testing for acceptance purposes.

5.2 End Point Measurements

5.2.1 A few characteristics only should be selected for each device category, which are of major importance for the specified device category. Recommended characteristics for various device categories are given in Table 3.

NOTE — Characteristics shall be measured in the sequence in which they are listed in Table 3, because the changes of characteristics caused by some failure mechanisms may be wholly or partially masked by the influence of other measurements.

5.2.2 All characteristics specified in Table 3 should be measured before and after life tests, unless otherwise specified in the relevant individual specification. Measurement of characteristics at the end of the test shall be made within 96 hours after completion of the test.

5.2.3 Measurements shall be made at an ambient temperature specified in **3.1**.

5.3 When only attributes analysis is planned, data may be taken by making measurements on a go/no-go basis (measured values are compared with specified limits, and the device is considered to be passed or failed). When variables analysis is planned, devices shall be individually identified and the value of each specified characteristic of each device shall be measured.

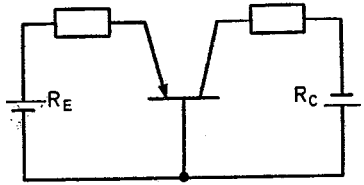
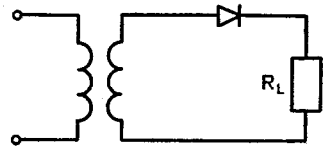
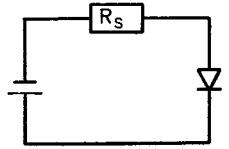
6. FAILURE CRITERIA

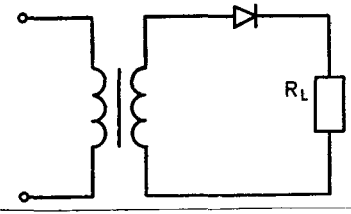
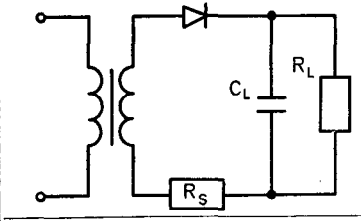
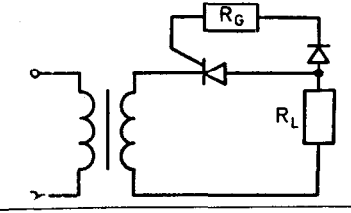
6.1 Each device which, after the life test, does not meet the limit specified for one or more of the characteristics for a device category, as given in Table 3 is considered to be a failure. In determining the failure the measurements may be referred to values measured at 25°C when necessary.

6.1.1 In presenting the failure data, the number of short-circuited and open-circuited devices should be given in addition to the total number of failures.

TABLE 1 DEVICE CATEGORIES AND ELECTRICAL STRESS CONDITIONS

(*Clauses* 3.5, 3.5.1 *and* 3.7)

Device Category	Test	Operating Conditions		Preferred Test Circuit	Remarks
		Current	Voltage		
Bipolar transistor	Operating life	$I_C = \frac{P_{tot\ Max}}{V_{CE}}$ (*see* Note 1)	$V_{CE} = 0{\cdot}7 V_{CEO\ Max}$ (*see* Note 2)	 (*see* Note 3)	$R_E \geqslant \frac{10 V_{EB}}{I_E}$ $R_C \approx \frac{V_{CB}}{I_C}$
Low-power signal diode	Operating life	Equivalent to a value which gives $P_{tot\ Max}$ power dissipation, or max specified average rectified current (*see* Note 4)	Sine wave 50-60 Hz, Peak value = $V_{R\ Max}$ specified		R_L = load resistor
Voltage reference diode and voltage regulator diode	Operating life	$I_{Z\ Max}$ as specified	Depends on I_Z		R_S = current limiting resistor $R_S \geqslant 0{\cdot}2 \left(\frac{V_Z}{I_Z} \right)$

Rectifier diode	Operating life (resistive load)	*see* **3.6**	Sine wave 50-60 Hz, peak value= 100% V_{RWM}		R_L = load resistor (*see* Note 5)
	Operating life (capacitive load)	Equivalent to the rated mean forward current for capacitive load	Sine wave 50-60 Hz, peak value= 100% V_{RWM}		C_L should have the highest capacitance specified R_S = current limiting resistor to be specified (*see* Note 5) R_L = load resistor
Thyristor	Operating life (resistive load)	*see* **3.6**	Sine wave 50-60 Hz, peak value= 100% V_{RWM} (or V_{DWM})		R_G = gate resistor R_L = load resistor (*see* Note 5)

NOTE 1 — $P_{tot\ Max}$ is the value of power dissipation corresponding to the temperature chosen in accordance with **3.4**.

NOTE 2 — Test conditions shall be within the safe operating area if one is specified. The voltage is to be lowered below 0·7 $V_{CEO\ Max}$ only as much as necessary to remain within the safe operating area.

NOTE 3 — Change circuit appropriately for npn transistor.

NOTE 4 — In cases where these values are not quoted in the data sheet, a value shall be specified for this test.

NOTE 5 — Alternatively a cheater circuit may be used.

NOTE 6 — Electrical stress conditions for integrated circuits are under consideration.

TABLE 2 DURATION OF LIFE TEST

(*Clause* 4.1)

Hours
$168 \begin{smallmatrix} +16 \\ -10 \end{smallmatrix}$
$336 \begin{smallmatrix} +16 \\ -20 \end{smallmatrix}$
$672 \begin{smallmatrix} +20 \\ -30 \end{smallmatrix}$
$1\,000 \begin{smallmatrix} +36 \\ -30 \end{smallmatrix}$
2 000
5 000 (*see* NOTE)
10 000 (*see* NOTE)

NOTE — Extended life tests for 5 000 and 10 000 hours may be carried out for evaluation of reliability of the devices which meet the conditions of life test as a type test.

7. PRECAUTIONS

7.1 Over-Temperature Controls of Ovens or Other Heat Sources — Devices may be destroyed or damaged if heat-source temperature controls fail during a test. It is recommended that heat sources should be equipped with redundant over-temperature controls, which are adjusted to limit maximum temperature to a value which will not destroy or damage the devices.

7.2 Oscillation Suppression and Current Limited

7.2.1 Active devices may be destroyed or damaged by oscillation while under test, at certain test conditions. The presence of harmful degrees of oscillations should be suitably detected (say by the use of a wide band oscilloscope) and the oscillations may be suppressed by adding shunt capacitance(s) and/or series inductance(s) and resistance(s) to the test circuits.

7.2.2 Devices may also be destroyed or damaged by thermal runaway occurring during a test. Device damage may be avoided by providing fixed resistance(s) which will limit the device dissipation during runaway. Such resistance(s) should be provided for each device, rather than for group of devices so that bias will not be removed from or reduced in all devices in a group, if one device runs away. When such resistance(s) are placed close to the device terminals, they will frequently function also as oscillation suppressor.

TABLE 3 DEVICE CATEGORIES, FAILURE CRITERIA AND FAILURE DEFINING CHARACTERISTICS

(*Clauses* 3.6.1, 5.2.1, 5.2.2 *and* 6.1)

Device Category	Characteristic	Failure Criteria	Ref to Note 1	Preferred Measurement Conditions
(1)	(2)	(3)	(4)	(5)
Bipolar transistor	I_{CBO}	$> 2 \times$ USL	USL	Highest V_{CB} specified for I_{CBO}
	h_{FE} (h_{fe}) (*see* Note 2)	$< 0{\cdot}8\ C \times$ LSL $> 1{\cdot}2 \times$ USL	LSL USL	A value of I_C, for which a h_{FE} (h_{fe}) tolerance (lower and upper limit) is specified
	V_{CEsat}	$> 1{\cdot}2 \times$ USL	USL	Highest I_C specified for V_{CEsat}
	$\mathcal{N}_F$ (*see* Note 3)	$>$ USL + 3dB	USL	Lowest I_C specified $\mathcal{N}_F$
Low power signal diode	I_R	$> 2 \times$ USL	USL	Highest V_R specified for I_R (*see* Note 4)
	V_F	$> 1{\cdot}1 \times$ USL	USL	Highest I_F specified for V_F
Voltage reference diode	I_R	$> 2 \times$ USL	USL	Highest V_R specified for I_R
	V_Z	$\lvert\triangle\rvert > 1\%$ (Note 5) $\lvert\triangle\rvert > 2\%$ (Note 6)	IVD	At specified I_Z for nominal V_Z
	r_z	$> 1{\cdot}2 \times$ USL	USL	—
	V_{nz}	$> 1{\cdot}5 \times$ USL	USL	*See* manufacturer's data sheet
Voltage regulator diode	I_R	$> 2 \times$ USL	USL	Highest V_R specified for I_R
	V_Z	$>$ USL $<$ LSL	USL LSL	At specified I_Z for nominal V_Z
	r_z	$> 1{\cdot}2 \times$ USL	USL	
Variable capacitance diode for tuning applications	I_R	$> 2 \times$ USL	USL	Highest V_R specified for I_R
	V_F	$> 1{\cdot}1 \times$ USL	USL	Highest I_F specified for V_F
	Q (*see* Note 7)	$< 0{\cdot}5 \times$ LSL	LSL	Lowest V_R specified for Q

(*Continued*)

TABLE 3 DEVICE CATEGORIES, FAILURE CRITERIA AND FAILURE DEFINING CHARACTERISTICS — *Contd*

Device Category	Characte-ristic	Failure Criteria	Ref to Note 1	Preferred Measure-ment Conditions
(1)	(2)	(3)	(4)	(5)
Rectifier diode	I_R	$> 2 \times$ USL	USL	Highest V_R ($= V_{RRM}$) and the highest temperature specified for I_R
	V_F	$> 1{\cdot}1 \times$ USL	USL	Highest I_F specified for V_F
Thyristor (*see* Note 8)	I_R	$> 2 \times$ USL	USL	Highest V_R ($=V_{RRM}$) and highest temperature specified for I_R
	V_T	$> 1{\cdot}1 \times$ USL	USL	Highest I_T specified for V_T
	I_{GT}	$> 1{\cdot}1 \times$ USL	USL	Lowest V_D specified for I_{GT}
	I_D	$> 2 \times$ USL	USL	Highest V_D ($=V_{DRM}$) and highest temperature specified for I_D

Note 1 — USL = Upper specification limit.
LSL = Lower specification limit.
IVD = Initial value of individual device.

Note 2 — Only where no h_{FE} tolerances are specified or where h_{FE} is unspecified.

Note 3 — Where applicable.

Note 4 — Where the V_R specified for I_R measurement is in the breakdown region, a lower value of V_R may be used.

Note 5 — For devices which are specified with a tolerance less than or equal to 1 percent.

Note 6 — For devices which are specified with a tolerance greater than 1 percent.

Note 7 — Replacement of Q by r_s is under consideration.

Note 8 — A thyristor is considered to have failed a test if it loses its ability to block the specified voltage during the test.

7.3 Miscellaneous

7.3.1 Adequate precautions shall be taken against damage by transients arising out of a single cause or combination of causes.

7.3.2 Adequate precautions shall also be taken to protect the devices against electrostatic voltages, electromagnetic fields and radio active fields.

8. SUMMARY

8.1 When this test is included in the relevant individual specification, the following shall be specified:

a) Mode of operation,
b) Mounting of the device,
c) Operating temperature,
d) Operating voltage,
e) Power dissipation or current and derating curve,
f) Appropriate test circuit and test conditions (*see* Table 1),
g) Duration (*see* Table 2),
h) Characteristics to be measured (*see* Table 3),
j) Failure criteria and failure limit (*see* Table 3), and
k) Any deviation from the procedure specified.

APPENDIX A

(*Clause* 0.3)

TYPE APPROVAL PROCEDURE FOR LIFE TESTING

A-1. GENERAL

A-1.1 Type testing to a given assurance level/acceptable quality level qualifies the product for all lower assurance levels/higher acceptable quality levels.

A-2. SELECTION OF SAMPLES

A-2.1 Unless otherwise specified, the number of samples shall be 10.

A-2.2 Samples shall be selected at random preferably from regular production lots so as to be as representative as possible of the type under consideration.

NOTE — *See* 3 of IS : 2612-1965* for details.

*Recommendation for type approval and sampling procedures for electronic components.

A-2.2.1 In case of failure, fresh samples not exceeding the original number may be called for to undergo the repeat test.

A-3. APPROVAL CRITERIA

A-3.1 The type shall be considered to satisfy the test and qualify for the type approval if no single failure has occurred.

A-3.2 In case of failure, repeat test(s) shall be conducted on samples selected in accordance with **A-2.2.1**. If in the repeat test(s), no single failure occurs, the type shall be considered to be eligible for approval, otherwise not.

APPENDIX B

(*Clause* 0.3)

ACCEPTANCE TEST PROCEDURE

B-1. SELECTION OF SAMPLES

B-1.1 Samples shall be selected at random from regular inspection lots so as to be representative of the type under consideration. For continuous production the samples may be selected in a regular periodic manner during manufacture.

NOTE — *See* 4 of IS : 2612-1965* for details.

B-1.2 The acceptance quality level (AQL) and the appropriate inspection level shall be specified in the relevant individual specification. The sampling procedure for acceptance of lot shall be corresponding to the specified AQL and inspection level in accordance with the procedure outlined in IS : 2612-1965* and/or IS : 2500 (Part I)-1973†.

B-1.2.1 Unless otherwise specified, for acceptance purpose, the AQL shall be 4 at an inspection level of IV.

B-2. APPROVAL/REJECTION CRITERIA

B-2.1 If the observed number of defectives exceeds the corresponding acceptance number for a specified AQL (*see* **B-1.2.1**), the lot shall be considered to have failed in the acceptance tests.

*Recommendation for type approval and sampling procedures for electronic components.

†Sampling inspection tables: Part I Inspection by attributes and by count of defects.

B-3. RESUBMISSION OF REJECTED LOTS

B-3.1 Rejected lots may, with the concurrence of the inspection authority, be resubmitted for inspection after all the components in the lot have gone through the tests in which there was failure and all the failing components have been removed or defects rectified. The inspection authority may also require that all components shall be subjected to such other specified tests as are independent of the test in which the lot failed and the failing components removed.

B-3.1.1 The resubmitted lots shall be inspected, using either normal or tightened inspection. Such lots may be inspected either for all tests or for same tests only if so agreed.

B-3.1.2 If the observed number of defectives in the resubmitted lot exceeds the corresponding acceptance number for the specified AQL the lot shall be considered failed in the acceptance tests.

INDIAN STANDARDS
ON
SEMICONDUCTOR DEVICES

IS:

1885 (Part VII) Electrotechnical vocabulary: Part VII Semiconductor devices,
- (Sec 1)-1970 General
- (Sec 2)-1970 Diodes
- (Sec 3)-1970 Transistors
- (Sec 4)-1969 Thyristors
- (Sec 5)-1971 Integrated circuits

2032 (Part VIII)-1965 Graphical symbols used in electrotechnology: Part VIII Semiconductor devices

3700 Essential ratings and characteristics of semiconductor devices:
- (Part I)-1972 General (*first revision*)
- (Part II)-1972 Low power signal diodes (*first revision*)
- (Part III)-1972 Rectifier diodes (*first revision*)
- (Part IV)-1968 Low power small signal transistors
- (Part V)-1968 Power transistors
- (Part VI)-1968 Switching transistors
- (Part VII)-1970 Reverse blocking triode thyristors
- (Part VIII)-1970 Voltage regulator and voltage reference diodes
- (Part IX)-1972 Variable capacitance diodes

3715 Letter symbols for semiconductor devices:
- (Part I)-1971 General aspects
- (Part II)-1971 Diodes
- (Part III)-1971 Transistors
- (Part IV)-1971 Thyristors

4400 Methods of measurements on semiconductor devices:
- (Part I)-1967 General
- (Part II)-1967 Low power signal diodes
- (Part III)-1968 Rectifier diodes
- (Part VII)-1971 Reverse blocking triode thyristors
- (Part VIII)-1970 Voltage regulator and voltage reference diodes

4411-1967 Code of designation of semiconducter devices

5000 Dimensions of semiconductor devices

NOTE — Standards on dimensions of semiconductor devices are published in loose leaf form (individually priced) and are supplied in an attractive binder (priced separately). So far 28 standards have been published.

5001 Guide for preparations of drawings of semiconductor devices and integrated circuits:
- (Part I) 1969 Semiconductor devices
- (Part II)-1973 Integrated circuits

5469 Code of practice for the use of semiconductor junction devices:
- (Prat I)-1969 Applicable to all devices
- (Part II)-1973 Diodes
- (Part III)-1973 Thyristors

6553-1971 Environmental requirements for semiconductor devices and integrated circuits

7412-1974 Life testing of semiconductor devices

PUBLICATIONS OF INDIAN STANDARDS INSTITUTION

INDIAN STANDARDS

Over 7 500 Indian Standards covering various subjects have been issued so far. Of these, the standards belonging to the Electrotechnical Group fall under the following categories:

Acoustics and acoustical measurement
Automobile electrical equipment
Batteries
Cinematographic equipment
Conductors and cables
Domestic electrical appliances
Electric welding equipment
Electrical installations, codes of practice
Electrical instruments
Electron tubes and valves
Electronic components
Electronic equipment
Environmental testing procedures
Fans
Flameproof electrical equipment
High voltage techniques
Illuminating engineering
Instrument transformers
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Lamps and lamp accessories
Lifts and escalators
Lightning arresters
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